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JC535 U.S. PTO 11/22/00

NEW PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Attorney Docket No. MLNR-07901

JC808 U.S. PTO 09/721555 11/22/00

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of Inventor: Gwilym Francis Luff et al.

Title: **INTEGRATED RADIO TRANSCEIVER**

CERTIFICATION UNDER 37 CFR § 1.10

I hereby certify that this New Application and the documents referred to as enclosed herein are being deposited with the United States Postal Service on this date, November 22, 2000, in an envelope bearing "Express Mail Post Office To Addressee" Mailing Label Number EL703161536US addressed to: **PATENT APPLICATION**, Assistant Commissioner for Patents, Washington, D.C. 20231.

Tadas Narauskas
(Name of Person Mailing Paper)

Tadas Narauskas
Signature

Enclosed are:

1. The papers required for filing date under CFR § 1.53(b):

   14 Pages of Specification (including claims); X Sheet(s) of Drawings.
   2 Formal
   1 Informal

2. X Declaration (combined with power of attorney) executed by Gwilym F. Luff
3. X Power of Attorney (combined with declaration) executed by Gwilym F. Luff
4. _ Assignment of the Invention to Micro Linear Corporation (including Form PTO-1595).
5. Fee Calculation

   _ Amendment changing number of claims or deleting multiple dependencies is enclosed

CLAIMS AS FILED

	Number Filed	Number Extra	Rate	Basic Fee
				$710 00
Total Claims	25 - 20 =	5	$18 00	90 00
Independent Claims	1 - 3 =	0	$80.00	0.00
Multiple Dependent claim(s), if any			$270 00	
			iling Fee Calculation	$800.00

6. X Applicants Qualify For Small Entity Status

   50% Filing Fee Reduction (if applicable) $400.00

7. Other Fees

   _ Assignment Recordation Fee

   __ Other 0 00

   TOTAL FEES ENCLOSED **$400.00**

7. Payment of Fees

   X Check in the amount of $400.00 enclosed.

8. X Authorization to Charge Additional Fees

   The Commissioner is hereby authorized to charge any additional fees (or credit any overpayment) associated with this communication and which may be required under 37 CFR § 1.16 or § 1.17 to Account No 08-1275. **An originally executed duplicate of this transmittal is enclosed for this purpose.**

9. __ Information Disclosure Statement
10. X Return Receipt Postcard

Dated. November 22, 2000

By: Thomas B. Haverstock
Name. Thomas B Haverstock
Registration No.: 32,571

PATENT
MLNR-07901

INTEGRATED RADIO TRANSCEIVER

RELATED APPLICATIONS:

This application claims priority under 35 U.S.C. § 119(e) of the co-pending U.S. provisional application Serial Number 60/167,195 filed on November 23, 1999 and entitled "Integrated Radio Transceiver."

FIELD OF THE INVENTION:

The present invention relates to an integrated radio transceiver. More particularly, the present invention relates to an integrated radio transceiver which maximizes the amount of common circuitry between a reception path, a transmission path and a frequency generator to increase the functionality of the transceiver with a low risk of interference.

BACKGROUND OF THE INVENTION:

A radio transceiver is a radio transmitter and receiver combined in one unit and having switching capabilities for selecting either the transmitting or receiving functions. The receiver combines the frequency of the received radio input signal with the frequency of a local oscillator to convert the radio signal to an intermediate frequency (IF) signal. The IF signal is then processed, filtered, and amplified. The transmitter portion of the transceiver filters, modulates and amplifies a signal to be transmitted.

An FM receiver including a phase-quadrature polyphase IF filter is disclosed in U.S. 5,715,529. The FM receiver includes circuitry incorporated in the signal path for converting a single-phase signal into a pair of signals in mutual phase quadrature. The IF device comprises a polyphase IF filter incorporated in the in-phase and quadrature signal paths and has a bandpass characteristic which is symmetrical around its resonance frequency. A low distortion selection of

an FM IF signal at a comparatively low intermediate frequency is easier to achieve with a polyphase filter than with a single-phase filter because the bandpass characteristic of a single-phase filter at lower values of the resonance frequency cannot be made symmetrical around the resonance frequency. In addition, the polyphase filter facilitates integration of the receiver onto a single chip since the requirement of using multiple single-phase filters is eliminated.

Signal processing within a conventional transceiver requires many components which cannot all be combined within one integrated circuit (IC). A voltage controlled oscillator (VCO) used for frequency generation is particularly difficult to implement on an IC because of the difficulty of making the VCO resonate with sufficient quality factor on the IC. Other components which cannot be implemented on the integrated circuit, such as filters and inductors, increase the cost and limit the functionality of the radio transceiver. For example, a radio transceiver with an unintegrated intermediate frequency filter can not operate beyond one intermediate frequency bandwidth. If only one bandwidth is used, the radio transceiver has either a receiver power or a performance disadvantage over multiple bandwidth implementations. This is due to the broader filter allowing the acceptance of more interference, i.e., signals entering the demodulator other than the desired signal such as signals from other transmitters and thermal noise. For broad band frequency operation, a conventional radio transceiver incorporates multiple oscillators to establish a number of different radio frequency channels resulting in a complex and costly circuit. Thus, an improved radio transceiver that can be incorporated within a single integrated circuit is desired.

SUMMARY OF THE INVENTION:

A radio transceiver in accordance with the present invention comprises a reception path, a transmission path, and a frequency generator with a programmable phase lock loop having an output coupled to the reception path and the transmission path. The reception path, the

transmission path, and the frequency generator share a maximum amount of common circuitry to facilitate implementation of the entire radio transceiver on a single integrated circuit. The transmission path can be controlled by either a modulated voltage controlled oscillator transmitter or an in-phase and quadrature modulator transmitter.

The reception path includes a radio frequency amplifier for amplifying a radio frequency input signal. Two equal in-phase signals are output from the radio frequency amplifier. An in-phase and quadrature radio frequency mixer combines the in-phase signals of the radio frequency amplifier with two in-phase and quadrature signals from the frequency generator and outputs in-phase and quadrature low intermediate frequency signals. The low intermediate frequency signals are input into an automatic gain control amplifier to extend the dynamic range of the low intermediate frequency signals. The signals of the reception path are then processed by a filter, an amplifier, and a demodulator prior to being received.

In accordance with one aspect of the present invention, the transmission path includes a transmission data filter and modulator for receiving data signals to be transmitted. A modulated voltage controlled oscillator receives a tuning input from a loop filter of the frequency generator and a modulation input from the transmission data filter and modulator. A programmable in-phase and quadrature divider receives a signal from the modulated voltage controlled oscillator and outputs two pairs of in-phase and quadrature signals. A transmission amplifier receives one of the signals from the divider and outputs a radio frequency signal to be transmitted. The programmable phase lock loop of the frequency generator receives another of the signals from the divider. The radio frequency mixer of the reception path receives one pair of the in-phase and quadrature signals from the divider.

In accordance with another aspect of the present invention, the transmission path of the radio transceiver comprises up-conversion mixers coupled to in-phase and quadrature signals output from the transmission data filter and modulator. The frequency generator includes a

voltage controlled oscillator coupled to the output of a loop filter. A programmable divider coupled with the output of the voltage controlled oscillator causes the programmable phase lock loop to produce a constant frequency at its output. An in-phase and quadrature divider is coupled to the output of the programmable divider and generates two pairs of in-phase and quadrature modulating signals. The up-conversion mixers are coupled with one pair of the modulating signals of the divider. A summer and a transmission amplifier combine and amplify the output signal of the up-conversion mixers to produce a modulated radio frequency output signal for transmission. The radio frequency mixer of the reception path receives the other pair of modulating signals from the divider. The programmable phase lock loop of the frequency generator is coupled to one of the outputs of the divider.

BRIEF DESCRIPTION OF THE DRAWINGS:

Figure 1 illustrates a block diagram of an integrated radio transceiver including a modulated voltage controlled oscillator transmitter.

Figure 2 illustrates a block diagram of an integrated radio transceiver including an in-phase and quadrature modulator transmitter.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS:

A block diagram illustrating a radio transceiver with a modulated voltage controlled oscillator (VCO) 2 transmitter implemented on a single integrated circuit (IC) in accordance with a preferred embodiment of the present invention is shown in Figure 1. The upper portion of the diagram illustrates a reception path of the radio transceiver. The lower portion of the diagram illustrates a transmission path of the radio transceiver. The central portion of the diagram illustrates a frequency generator of the radio transceiver.

A radio frequency (RF) input signal is input into an RF amplifier 4. The output of the RF

amplifier 4 is divided into two equal in-phase signals. The in-phase signals are input into an in-phase and quadrature (IQ) RF mixer 6. IQ local oscillator (LO) signals from the frequency generator are also input into the RF mixer 6. A low intermediate frequency (IF) signal is output from the RF mixer 6 and coupled to an automatic gain control (AGC) amplifier 8. The output of the AGC amplifier 8 is sent to an IQ IF filter 10. The output of the IF filter 10 is input into an IF amplifier 12 before being demodulated by a demodulator 14. The demodulator 14 outputs the signals to be received.

Data signals to be transmitted enter a transmission data filter and modulator 16. The output of the filter/modulator 16 is coupled with the input of the VCO 2. The output of the VCO 2 is fed to a programmable divider 18. The output of the programmable divider 18 is coupled to an IQ divider 20. The output of the IQ divider 20 is amplified via a transmission amplifier 22. An RF signal is output from the transmission amplifier 22.

The frequency generator of the radio transceiver comprises a programmable phase lock loop (PLL) 24 having an output coupled to a loop filter 26. The output of the loop filter 26 is fed to the input of the VCO 2. The output of the VCO 2 is coupled to the programmable divider 18. The output of the programmable divider 18 is input into the IQ divider 20. The dual outputs of the IQ divider 20 are coupled to the RF mixer 6. One of the dual outputs of the IQ divider 20 is fed back to the programmable PLL 24.

A control interface 28 is coupled with the AGC amplifier 8, the IF amplifier 12, the demodulator 14, the programmable PLL 24, and the filter/modulator 16.

The RF operating channel is determined by the VCO frequency and the division ratio provided by the dividers 18, 20. The RF input signal is amplified by the RF amplifier 4 and divided into two equal in-phase signals. The in-phase signals are coupled with the RF mixer 6 which is also fed with the IQ LO signals from the IQ divider 20. The signals output from the RF mixer 6 have a center IF frequency less than the RF channel separation frequency. Typical

values for RF channel separation in digital cordless and cellular telephones are in the 100kHz to 2MHz range. For wireless data applications, the range could be greater than 10MHz. The RF mixer 6 removes signals at the image frequency thereby eliminating the need for an RF filter. The signals output from the RF mixer 6 are combined in the IF filter 10. The AGC amplifier 8 between the RF mixer 6 and the IF filter 10 extends the dynamic range of the IF signal. To further increase the dynamic range of the IF signal or lower the interference sensitivity of the reception path, additional filters and amplifiers can be used.

After the IF filter 10, the IF amplifier 12 which may be a limiter or an AGC amplifier increases the IF signal level before being processed by the demodulator 14. The demodulator 14 may be a discriminator and data slicer, a discriminator with the output fed to an analog-to-digital converter (ADC) and then demodulated off the IC, digitizing the IF filter 10 outputs using ADCs then demodulating off the IC, or digitizing the IF filter 10 outputs using ADCs then demodulating on the IC. One implementation of the demodulator 14 is to integrate a pulse counting discriminator where the IF amplifier 12 comprises two identical limiter circuits. Since the output of the limiters are in phase and quadrature, an IQ circuit in the discriminator is not required. A data filter is used after the discriminator to remove the IF products and limit the noise bandwidth. A data slicer after the discriminator converts an analog signal to a digital signal. The data slicer is a comparator having a first input coupled with the output of the data filter and a second input being a time averaged version of this signal. The low IF reception path enables a reduction in RF filters and removal of conventional IF filters.

The radio transceiver of the present invention is intended for half duplex radios and receivers. Such radios and receivers cannot simultaneously receive and transmit signals. The RF input channel frequency can be either the same or different than the frequency of the transmitted output signal. The preferred radio transceiver operates on different RF channels. The operating RF is determined by the VCO 2 frequency and the division ratio of the dividers 18, 20. The

VCO 2 frequency is controlled by the programmable PLL 24 which phase locks the VCO 2 to a stable reference frequency source such as a crystal oscillator. The VCO 2 is related to the reference frequency source by the division ratio. The VCO 2 receives a tuning input from the loop filter 26 and a modulation input from the transmission data filter/modulator 16. FM modulation is performed by applying a modulating voltage to the VCO 2. After the VCO 2 is modulated, either the IQ or LO signal is fed to the transmission amplifier 22. Increasing the programmable divider 18 value increases the division ratio thereby enabling the VCO 2 to ensure signal isolation during transmission.

The programmable divider 18 enables the use of a single VCO 2 while allowing the radio transceiver to operate over a very wide frequency range. For cellular telephones dual radio frequency band operation is typically required at 900MHz and 1900MHz. These values vary depending on the government region, e.g. U.S., Europe, and Japan. Another application of the integrated radio transceiver of the present invention relates to RF reduction converters for cable, terrestrial and satellite TV services which utilize multiple VCOs for covering frequency bands between 10MHz and 2GHz. Since only one VCO 2 is required in the integrated radio transceiver of the present invention, the most efficient use of space on the IC is promoted.

Integration of the IF filter 10 onto a single IC enables the radio transceiver to operate at more than one IF bandwidth and can be achieved using either different IF filters 10 with different bandwidths or switching circuits within one IF filter 10 to change the bandwidth. Such a technique can be applied for both reception and transmission. This is significantly beneficial for multiple standard radios, e.g. a combined cellular and cordless telephone, which require different operational bandwidths. Generally, if only one bandwidth is used, the radio transceiver has either a receiver power or performance disadvantage over multiple bandwidth implementation since the broader filter admits more interference. For broad band frequency operation, an N value (integer number>0) of the programmable divider 18 can be selected to allow for an octave

or greater operating RF range with the same VCO 2 thereby reducing circuit complexity and cost.

Automatic tuning of the IF filter 10 is achieved by generating a calibration signal at the IF center frequency using the programmable PLL 24 reference frequency. The center frequency of the IF filter 10 can be automatically adjusted when the programmable PLL 24 is locking prior to reception or transmission to remove process and temperature variations. This eliminates the need for either adjustment in the radio manufacture/test stages or the IC manufacture/test stages.

In addition to the RF transceiver circuit, high speed logic circuits could be incorporated on the IC to address other functions. The clock frequency will typically be multiples of the IF frequency, thus interference will be generated at a higher frequency than the IF frequency. This enables the integration of highly sensitive receiver circuits with logic and signal processing digital circuits.

Figure 2 illustrates a block diagram of the transceiver having an IQ modulator transmitter. This configuration is essentially identical to the block diagram shown in Figure 1 except that an alternative modulation scheme is employed where the VCO 2 frequency is not varied. The output of the loop filter 26 is the only input of VCO 2. The output of the VCO 2 is fed to the dividers 18, 20 whereby the programmable PLL 24 produces a constant frequency at its output. The IQ divider 20 generates IQ modulating signals for transmission. The data transmission signals are input into the transmission data filter/modulator 16. IQ signals are output from the filter/modulator 16 and are combined with the IQ modulating signals from the IQ divider 20 in up-conversion mixers 30. The output of the up-conversion mixers 18 are combined by a summer 32 and amplified by the transmission amplifier 22 to produce the modulated RF output signal to be transmitted. The IQ divider 20 utilizes either a baseband modulation signal (DC signal content) or an IQ IF signal at the same frequency as the IF. For a time division duplex radio that transmits on the same RF frequency as it receives, switching the frequency of the VCO 2

between transmit and receive is not required.

The above description of the integrated radio transceiver in accordance with the present invention discloses a single programmable phase lock loop shared by both reception and transmission paths. Such a configuration allows all of the components of the radio transceiver to be integrated on a single IC which heretofore has never been accomplished. Thus, the integrated radio transceiver in accordance with the present invention is novel and unobvious and should be granted a patent on the merits.

The present invention has been described in terms of specific embodiments incorporating details to facilitate the understanding of the principles of construction and operation of the invention. Such reference herein to specific embodiments and details thereof is not intended to limit the scope of the claims appended hereto. It will be apparent to those skilled in the art that modifications can be made in the embodiment chosen for illustration without departing from the spirit and scope of the invention. Specifically, it will be apparent to one of ordinary skill in the art that the device of the present invention could be implemented in several different ways and the architecture, system and method disclosed above are only illustrative of preferred embodiments of the invention.

CLAIMS

We Claim:

1. A radio transceiver comprising:

a reception path;

a transmission path; and

a frequency generator comprising a programmable phase lock loop having an output coupled to the reception path and the transmission path;

wherein the reception path, the transmission path, and the frequency generator share a maximum amount of common circuitry to facilitate implementation of the entire radio transceiver on a single integrated circuit.

2. The radio transceiver as claimed in Claim 1, wherein the reception path includes a radio frequency amplifier for amplifying a radio frequency input signal, the output of the radio frequency amplifier being divided into two equal in-phase signals.

3. The radio transceiver as claimed in Claim 2, wherein the reception path includes an in-phase and quadrature radio frequency mixer for receiving the in-phase signals of the radio frequency amplifier.

4. The radio transceiver as claimed in Claim 3, wherein the radio frequency mixer of the reception path receives in-phase and quadrature signals from the frequency generator and outputs in-phase and quadrature low intermediate frequency signals.

5. The radio transceiver as claimed in Claim 4, wherein the reception path includes an

automatic gain control amplifier receiving the low intermediate frequency signals output from the radio frequency mixer for extending the dynamic range of the intermediate frequency signals.

6. The radio transceiver as claimed in Claim 5, wherein the reception path includes an in-phase and quadrature intermediate frequency filter coupled with the output of the automatic gain control amplifier.

7. The radio transceiver as claimed in Claim 6, wherein the reception path includes an intermediate frequency amplifier coupled with the output of the intermediate frequency filter.

8. The radio transceiver as claimed in Claim 7, wherein the reception path includes a demodulator coupled with the output of the intermediate frequency amplifier.

9. The radio transceiver as claimed in Claim 1, wherein the transmission path includes a transmission data filter and modulator for receiving data signals to be transmitted.

10. The radio transceiver as claimed in Claim 9, wherein the transmission path includes a modulated voltage controlled oscillator receiving a tuning input from the frequency generator and a modulation input from the transmission data filter and modulator.

11. The radio transceiver as claimed in Claim 10, wherein the frequency generator includes a loop filter receiving an input signal from the programmable phase lock loop and providing the voltage controlled oscillator with the tuning input.

12. The radio transceiver as claimed in Claim 10, wherein the transmission path includes a

programmable divider coupled with the output of the modulated voltage controlled oscillator.

13. The radio transceiver as claimed in Claim 12, wherein the transmission path includes an in-phase and quadrature divider receiving the output of the programmable divider and outputting in-phase and quadrature signals.

14. The radio transceiver as claimed in Claim 13, wherein the transmission path includes a transmission amplifier receiving one signal output from the in-phase and quadrature divider, the output of the transmission amplifier being a radio frequency signal to be transmitted.

15. The radio transceiver as claimed in Claim 14, wherein the programmable phase lock loop of the frequency generator receives one signal output from the in-phase and quadrature divider.

16. The radio transceiver as claimed in Claim 13, wherein the radio frequency mixer of the reception path receives the in-phase and quadrature signals from the in-phase and quadrature divider.

17. The radio transceiver as claimed in Claim 9, wherein the transmission path includes up-conversion mixers coupled to in-phase and quadrature signals output from the transmission data filter and modulator.

18. The radio transceiver as claimed in Claim 17, wherein the frequency generator includes a loop filter receiving an input signal from the programmable phase lock loop and transmitting a signal to a voltage controlled oscillator.

19. The radio transceiver as claimed in Claim 18, wherein the frequency generator includes a programmable divider coupled with the output of the voltage controlled oscillator whereby the programmable phase lock loop produces a constant frequency at its output.

20. The radio transceiver as claimed in Claim 19, wherein the frequency generator includes an in-phase and quadrature divider coupled to the output of the programmable divider and generating in-phase and quadrature modulating signals for transmission.

21. The radio transceiver as claimed in Claim 20, wherein the up-conversion mixers are coupled with the modulating signals of the in-phase and quadrature divider.

22. The radio transceiver as claimed in Claim 21, wherein the transmission path includes a summer for combining the signal output of the up-conversion mixers.

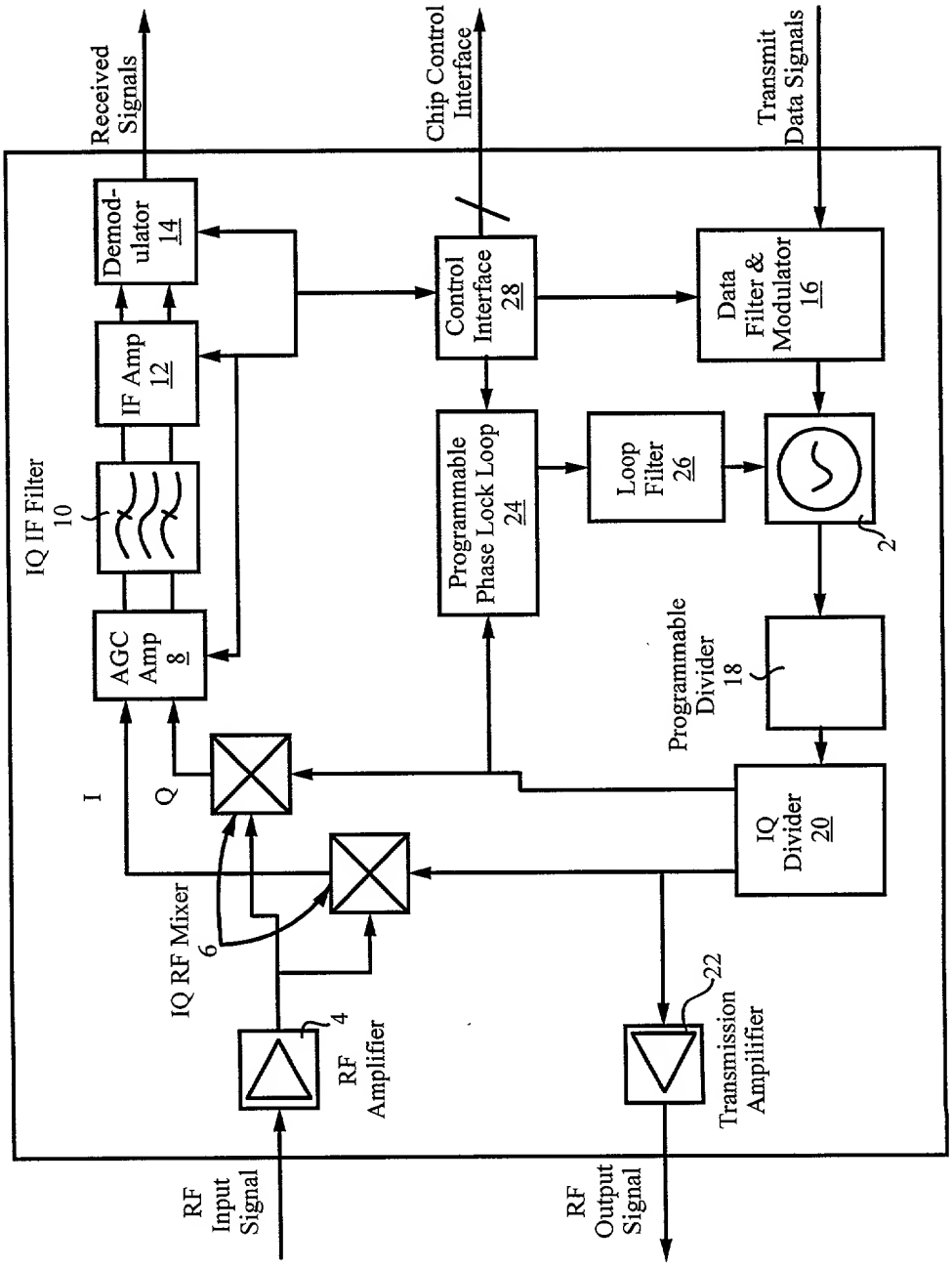
23. The radio transceiver as claimed in Claim 22, wherein the transmission path includes a transmission amplifier coupled with the output of the summer to produce the modulated radio frequency output signal for transmission.

24. The radio transceiver as claimed in Claim 9, wherein the programmable phase lock loop of the frequency generator receives a signal output from the in-phase and quadrature divider.

25. The radio transceiver as claimed in Claim 9, wherein the radio frequency mixer of the reception path receives output signals from the in-phase and quadrature divider.

ABSTRACT

A radio transceiver comprises a reception path, a transmission path, and a frequency generator with a programmable phase lock loop. The reception path, the transmission path, and the frequency generator share a maximum amount of common circuitry to facilitate implementation of the entire radio transceiver on a single integrated circuit. The reception path includes an amplifier and a quadrature mixer for producing low intermediate frequency signals. The transmission path can be controlled by either a modulated voltage controlled transmitter or an in-phase and quadrature modulator transmitter.



Block Diagram of Transceiver with Modulated VCO Transmitter

Fig. 1

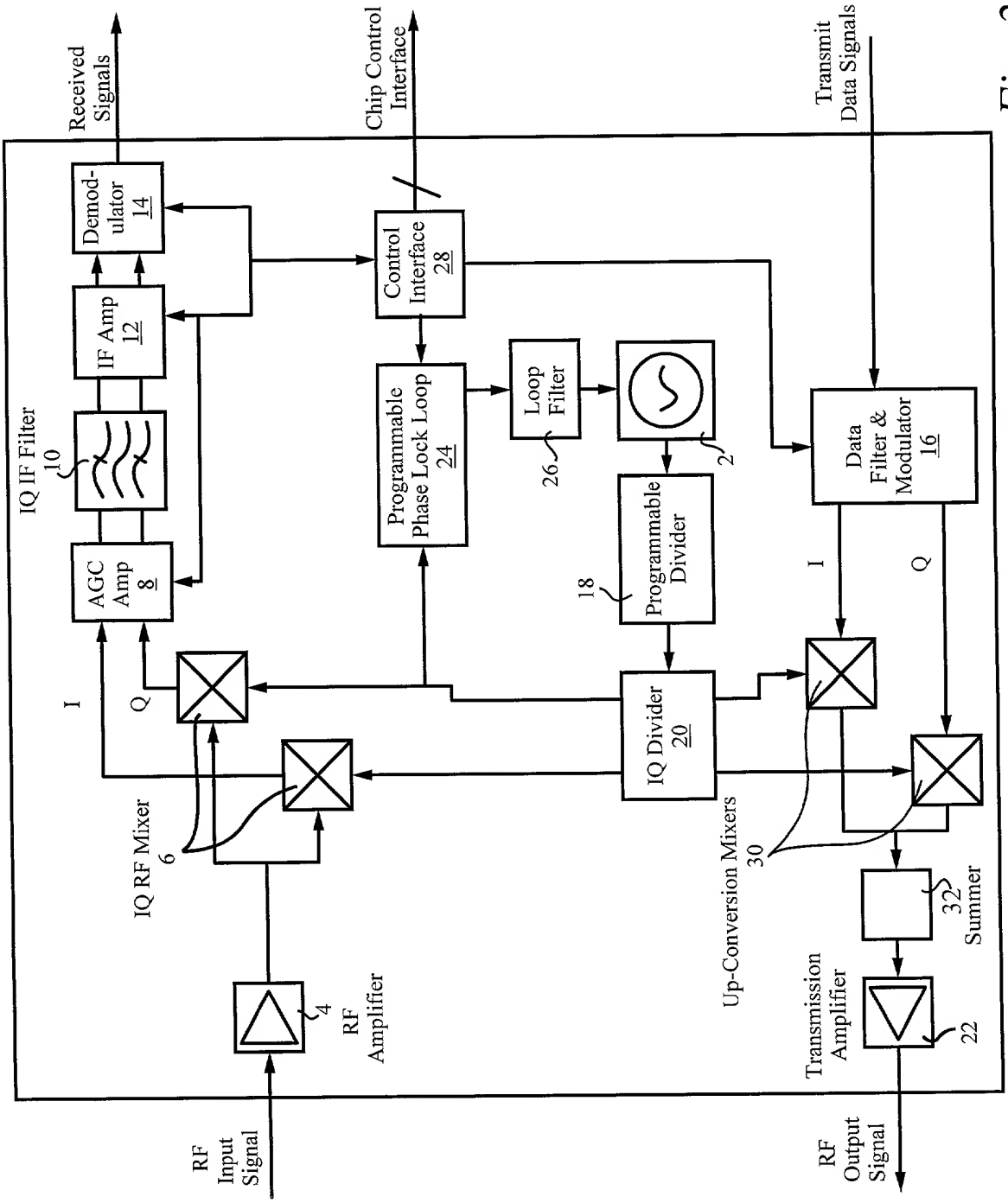


Fig. 2

Block Diagram of Transceiver with IQ Modulator Transmitter

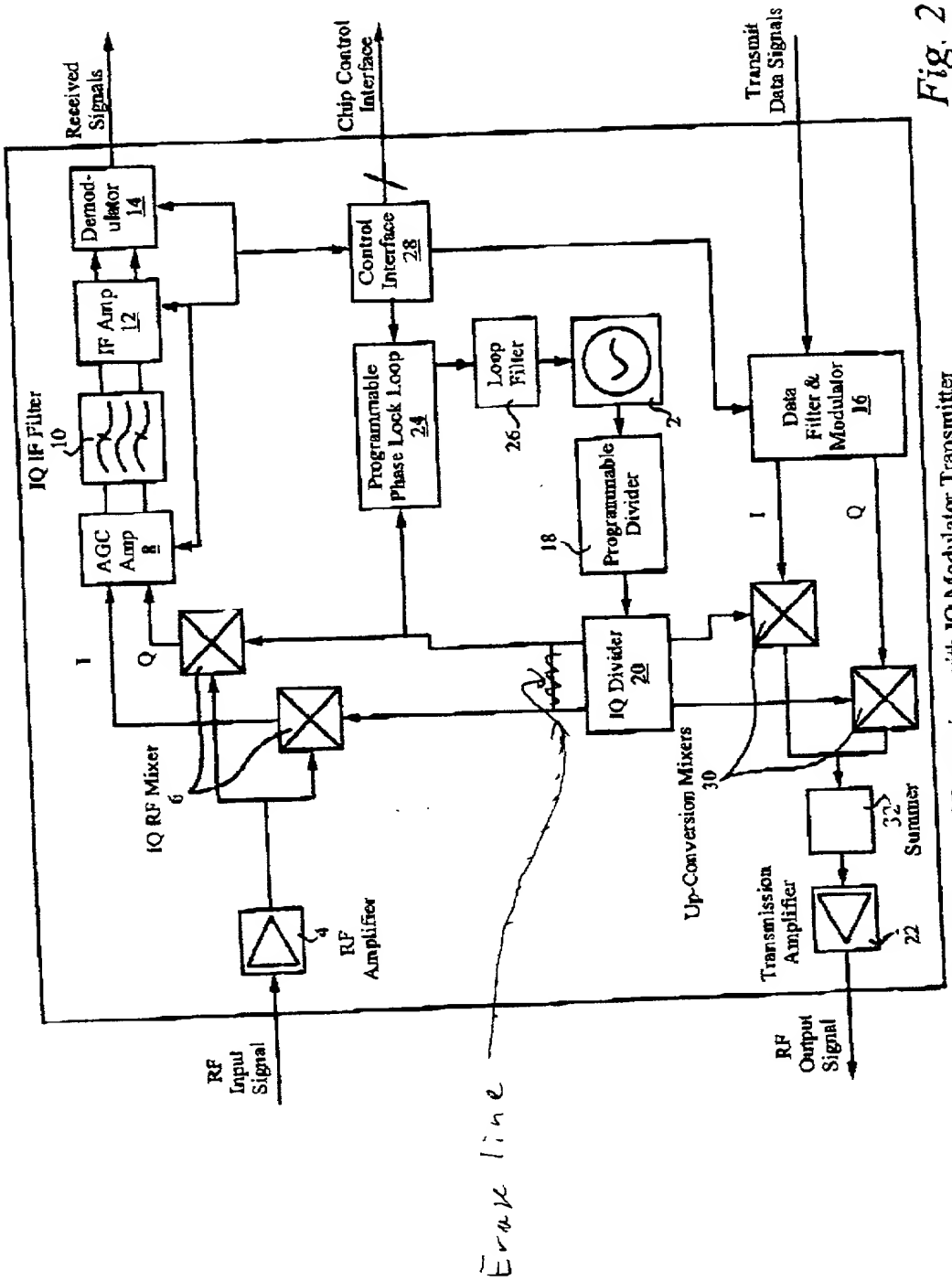


Fig. 2
Black Diagram of Transceiver with IQ Modulator Transmitter

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PATENT
Attorney Docket No.: MI NR-07901

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name. I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **INTEGRATED RADIO TRANSCEIVER**. The specification of which is attached hereto. I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claim	
			Yes	No
Number	Country	Day/Month/Year Filed		

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status: Patented, Pending, Abandoned

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

60/167,195	November 23, 1999
Application Serial No.	Filing Date

I hereby appoint the following as my attorneys with full power of substitution to prosecute this application and transact all business in the Patent and Trademark Office in connection therewith:

Thomas B. Haverstock	32,571	Jonathan O. Owens	37,902

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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